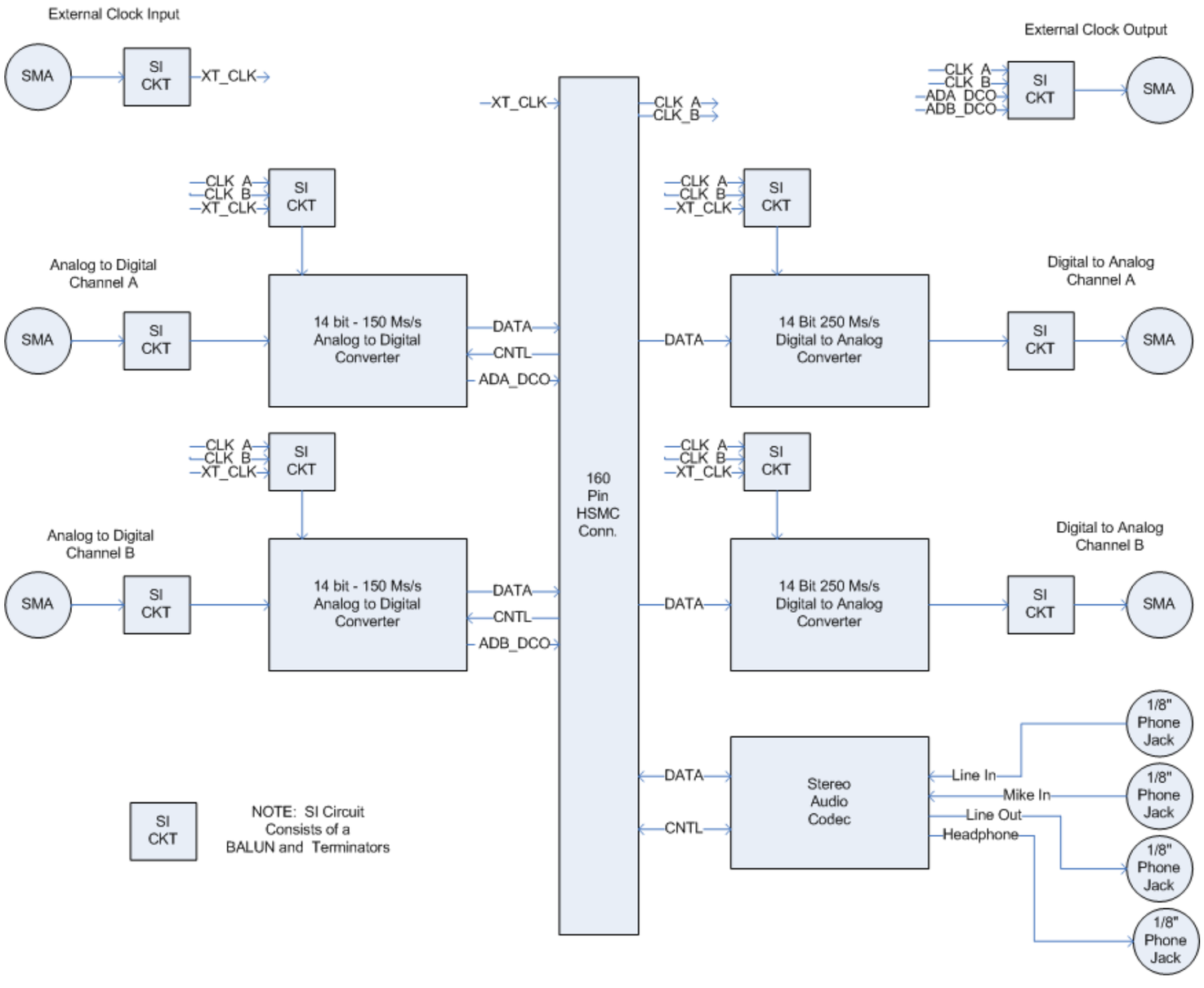

Note: Unused shunts should accompany board in kit, packaged in a separate bag for user re-configuration

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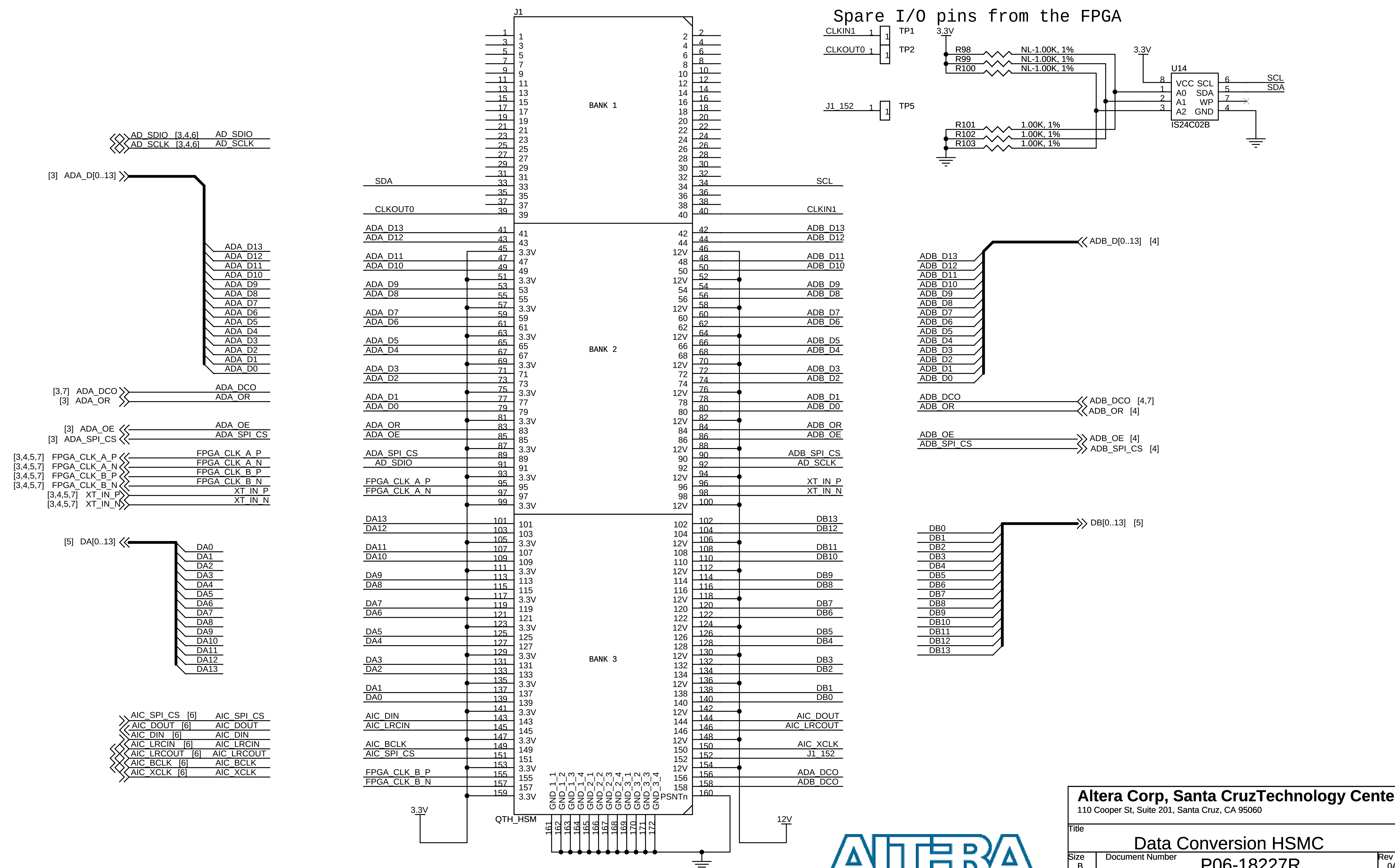

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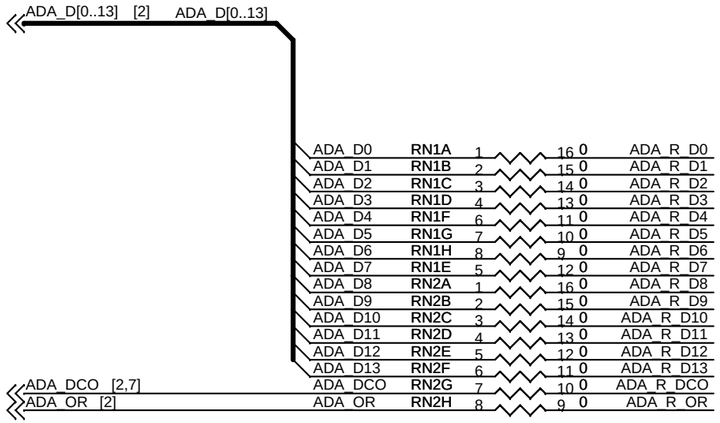
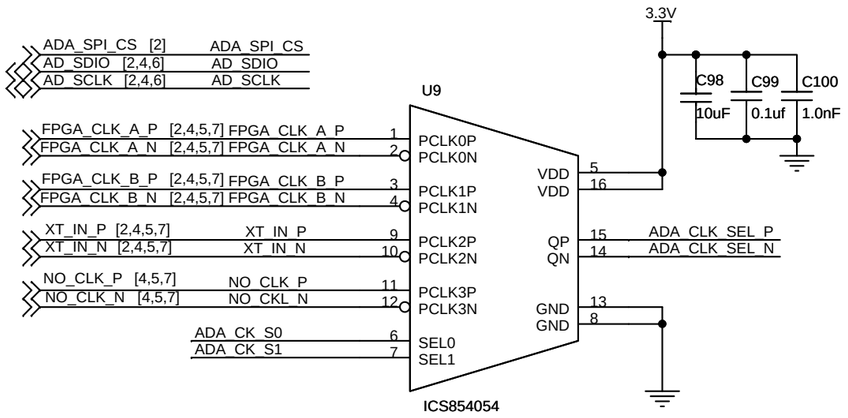
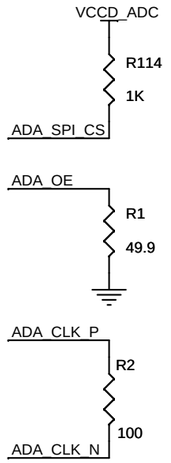
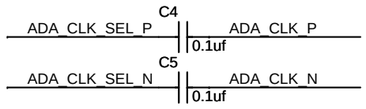
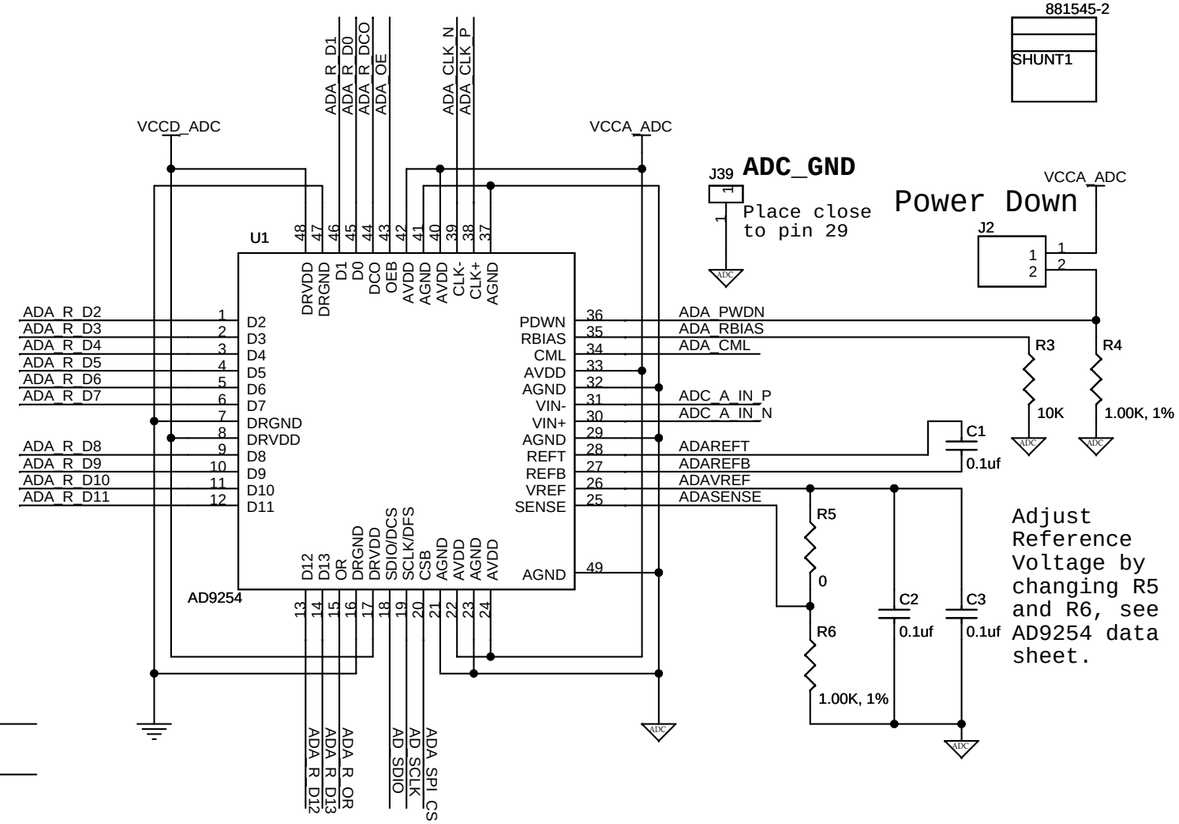
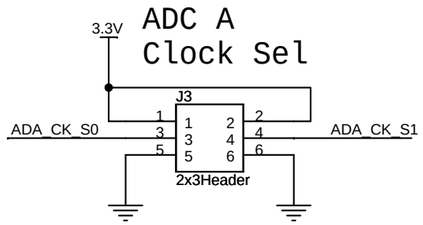


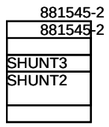






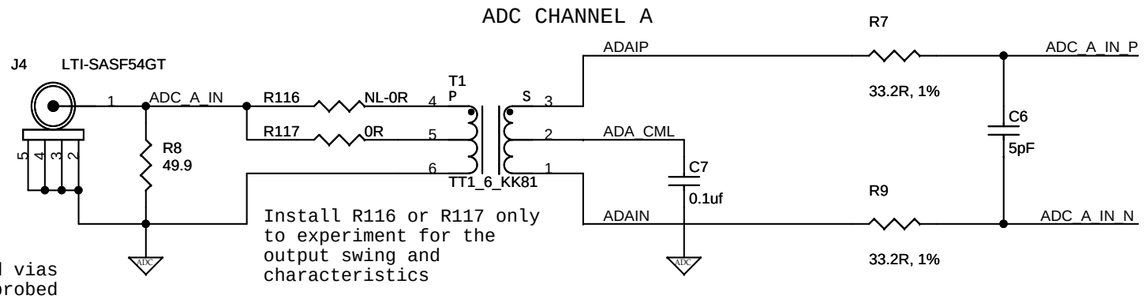






Clock Configuration

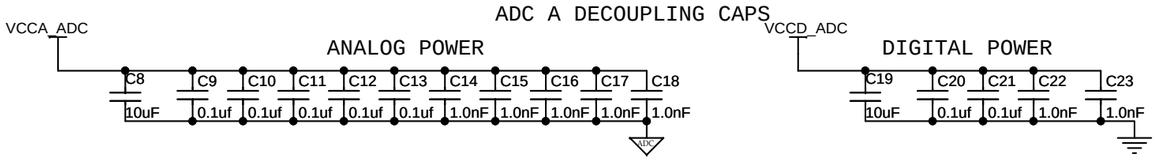
Clock	Jumpers on...
FPGA A	3-5,4-6
FPGA B	1-3,4-6
EXT	3-5,2-4
NONE	1-3,2-4



Place R8 on top layer with untented vias so that it can be probed for testing puroses.

Analog to Digital Converter Channel A

14 Bit, 150 Ms/s, Analog Devices AD9254



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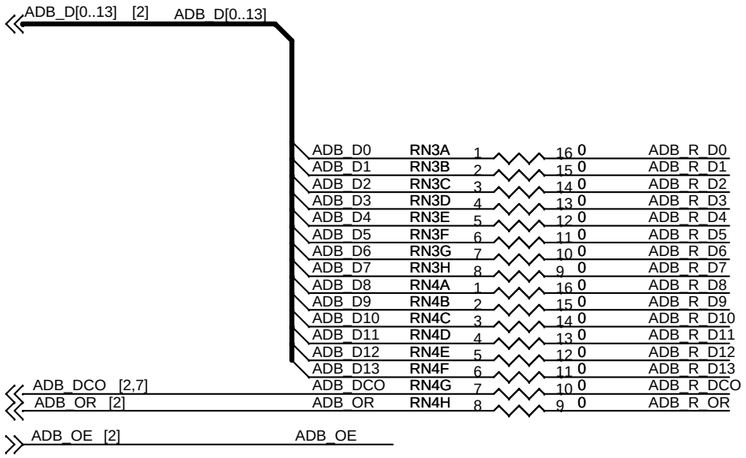
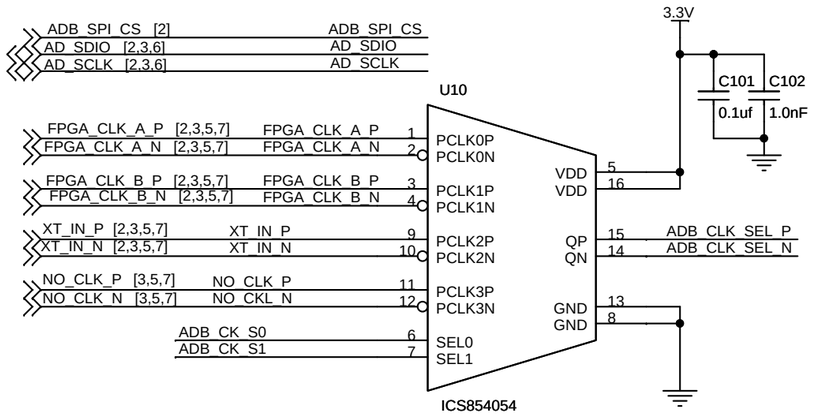
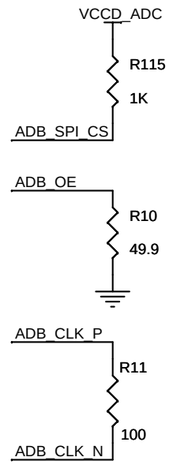
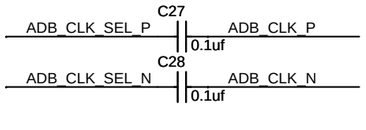
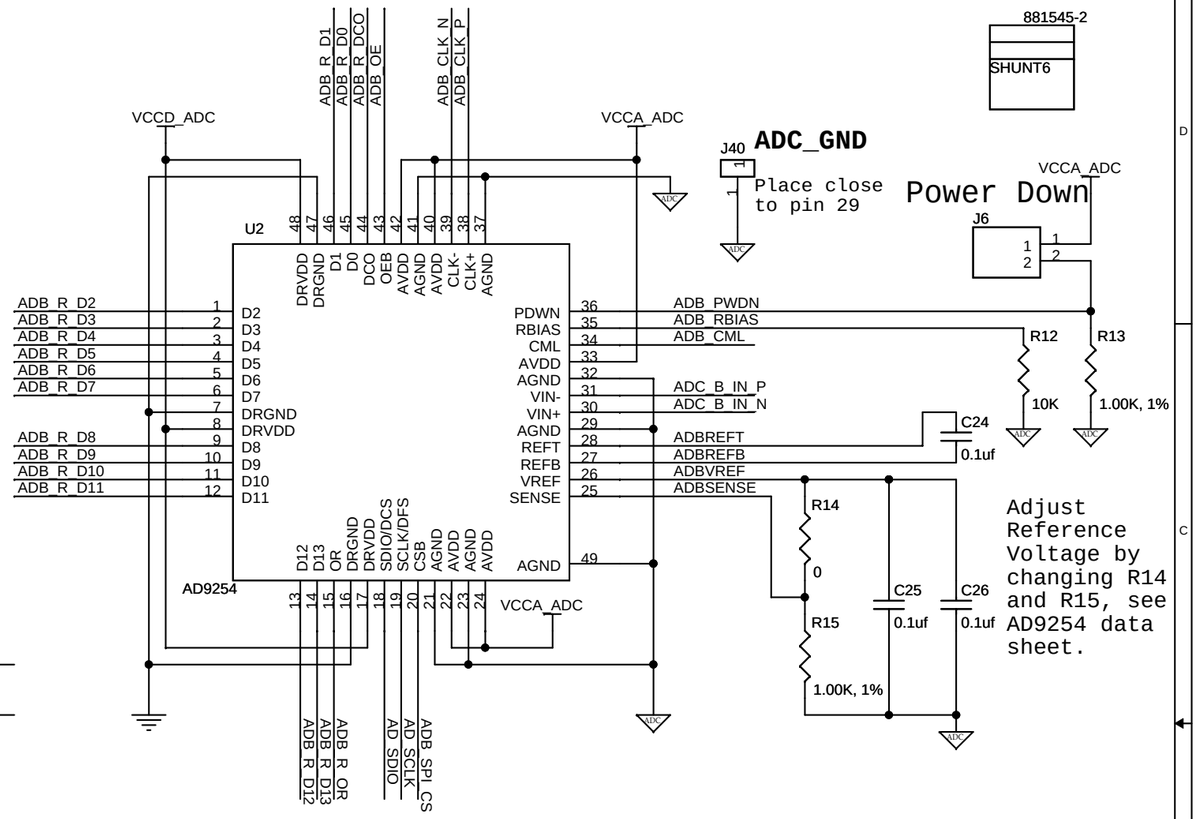


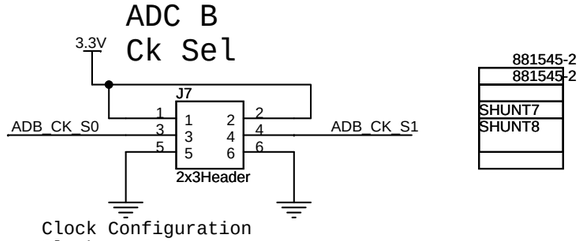








Adjust Reference Voltage by changing R14 and R15, see AD9254 data sheet.

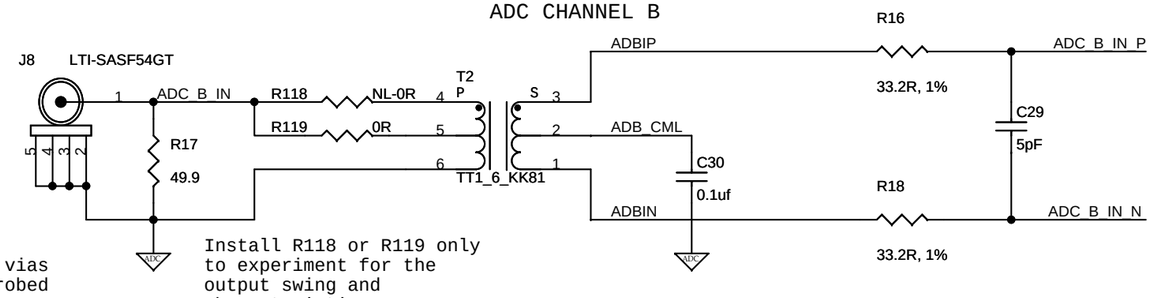


Clock Configuration

Clock	Jumpers on...
FPGA A	3-5,4-6
FPGA B	1-3,4-6
EXT	3-5,2-4
NONE	1-3,2-4

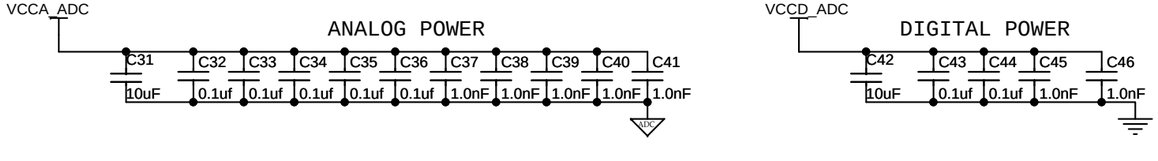
Place R17 on top layer with untented vias so that it can be probed for testing puroses.

ADC CHANNEL B



Install R118 or R119 only to experiment for the output swing and characteristics

ADC B DECOUPLING CAPS



Analog to Digital Converter Channel B

14 Bit, 150 Ms/s, Analog Devices AD9254

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881545-2
881545-2
SHUNT16
SHUNT17

Clock Configuration

Clock	Jumpers on...
FPGA A	3-5,4-6
FPGA B	1-3,4-6
EXT	3-5,2-4
NONE	1-3,2-4

DAC A Ck Sel

3.3V
J15
DAA_CK_S0
DAA_CK_S1
2x3Header

881545-2
881545-2
SHUNT11
SHUNT12
SHUNT13

J10 GSET
J11 MODE
J13 SLEEP
VCCA_DAC

U3
DAC_GSET 42 → GSET
DAC_MODE 48 → MODE
DAC_SLEEP 37 → SLEEP
17 WRTA/WRTIQ
20 WRTB/SELECTIQ
18 CLKA/CLKIQ
19 CLKB/RESETIQ
AVDD 47
DVDD 16
DVDD 22
DAC5672IPFBR

C47 10pf, C48 10pf, C49 0.1uf, C50 0.1uf
C51 10pf, C52 10pf, C53 0.1uf, C54 0.1uf

DA[0..13] [2]
DB[0..13] [2]

DA0	DA0	14	DA0
DA1	DA1	13	DA1
DA2	DA2	12	DA2
DA3	DA3	11	DA3
DA4	DA4	10	DA4
DA5	DA5	9	DA5
DA6	DA6	8	DA6
DA7	DA7	7	DA7
DA8	DA8	6	DA8
DA9	DA9	5	DA9
DA10	DA10	4	DA10
DA11	DA11	3	DA11
DA12	DA12	2	DA12
DA13	DA13	1	DA13
DB0	DB0	36	DB0
DB1	DB1	35	DB1
DB2	DB2	34	DB2
DB3	DB3	33	DB3
DB4	DB4	32	DB4
DB5	DB5	31	DB5
DB6	DB6	30	DB6
DB7	DB7	29	DB7
DB8	DB8	28	DB8
DB9	DB9	27	DB9
DB10	DB10	26	DB10
DB11	DB11	25	DB11
DB12	DB12	24	DB12
DB13	DB13	23	DB13

BIASJ_A 44 DAC_A_BIAS
IOUTA1 46 DAC_A_OUT1
IOUTA2 45 DAC_A_OUT2
R104 0 2K R23

BIASJ_B 41 DAC_B_BIAS
IOUTB1 39 DAC_B_OUT1
IOUTB2 40 DAC_B_OUT2
EXTIO 43
R105 0 2K R26
DAC_REF
C55 0.1uf

AGND 38
DGND 15
DGND 21

J41 DAC_GND
Place close to output pins

Install R120 or R121 only to experiment for the output swing and characteristics

DAC_A_OUT1
R19 49.9
R20 100
DAC_A_OUT2
R21 49.9
T3 TT1_6_KK81
R120 NL-0R
R121 0R
LTI-SASF54GT J12
DAC_A_1

Place R20 and R24 on top layer with untented vias so that it can be probed for testing puroses.

Install R122 or R123 only to experiment for the output swing and characteristics

DAC_B_OUT1
R22 49.9
R24 100
DAC_B_OUT2
R25 49.9
T4 TT1_6_KK81
R122 NL-0R
R123 0R
LTI-SASF54GT J14
DAC_B_1

U11
FPGA_CLK_A_P [2,3,4,7] → FPGA_CLK_A_P → PCLK0P (1)
FPGA_CLK_A_N [2,3,4,7] → FPGA_CLK_A_N → PCLK0N (2)
FPGA_CLK_B_P [2,3,4,7] → FPGA_CLK_B_P → PCLK1P (3)
FPGA_CLK_B_N [2,3,4,7] → FPGA_CLK_B_N → PCLK1N (4)
XT_IN_P [2,3,4,7] → XT_IN_P → PCLK2P (9)
XT_IN_N [2,3,4,7] → XT_IN_N → PCLK2N (10)
NO_CLK_P [3,4,7] → NO_CLK_P → PCLK3P (11)
NO_CLK_N [3,4,7] → NO_CLK_N → PCLK3N (12)
DAA_CK_S0 → SEL0 (6)
DAA_CK_S1 → SEL1 (7)
VDD (5, 16)
GND (13, 8)
QP → DAC_CLK_1_P (15)
QN → DAC_CLK_1_N (14)
C103 0.1uf, C104 1.0nF
ICS854054

U12
FPGA_CLK_A_P [2,3,4,7] → FPGA_CLK_A_P → PCLK0P (1)
FPGA_CLK_A_N [2,3,4,7] → FPGA_CLK_A_N → PCLK0N (2)
FPGA_CLK_B_P [2,3,4,7] → FPGA_CLK_B_P → PCLK1P (3)
FPGA_CLK_B_N [2,3,4,7] → FPGA_CLK_B_N → PCLK1N (4)
XT_IN_P [2,3,4,7] → XT_IN_P → PCLK2P (9)
XT_IN_N [2,3,4,7] → XT_IN_N → PCLK2N (10)
NO_CLK_P [3,4,7] → NO_CLK_P → PCLK3P (11)
NO_CLK_N [3,4,7] → NO_CLK_N → PCLK3N (12)
DAB_CK_S0 → SEL0 (6)
DAB_CK_S1 → SEL1 (7)
VDD (5, 16)
GND (13, 8)
QP → DAC_CLK_2_P (15)
QN → DAC_CLK_2_N (14)
C105 0.1uf, C106 1.0nF
ICS854054

U4
DAC_CLK_1_N (1)
DAC_CLK_1_P (2)
DAC_CLK_2_P (3)
DAC_CLK_2_N (4)
VCC (8)
CLKA (7)
CLKB (6)
GND (5)
FIN1028

DA0	R27	NL-49.9	
DA1	R29	NL-49.9	
DA2	R31	NL-49.9	
DA3	R33	NL-49.9	
DA4	R35	NL-49.9	
DA5	R37	NL-49.9	
DA6	R39	NL-49.9	
DA7	R41	NL-49.9	
DA8	R43	NL-49.9	
DA9	R45	NL-49.9	
DA10	R47	NL-49.9	
DA11	R49	NL-49.9	
DA12	R51	NL-49.9	
DA13	R53	NL-49.9	
CLKA	R55	NL-49.9	

DB0	R28	NL-49.9	
DB1	R30	NL-49.9	
DB2	R32	NL-49.9	
DB3	R34	NL-49.9	
DB4	R36	NL-49.9	
DB5	R38	NL-49.9	
DB6	R40	NL-49.9	
DB7	R42	NL-49.9	
DB8	R44	NL-49.9	
DB9	R46	NL-49.9	
DB10	R48	NL-49.9	
DB11	R50	NL-49.9	
DB12	R52	NL-49.9	
DB13	R54	NL-49.9	
CLKB	R56	NL-49.9	

DAC B Ck Sel

3.3V
J17
DAB_CK_S0
DAB_CK_S1
2x3Header

881545-2
881545-2
SHUNT14
SHUNT15

Clock Configuration

Clock	Jumpers on...
FPGA A	3-5,4-6
FPGA B	1-3,4-6
EXT	3-5,2-4
NONE	1-3,2-4

ALTERA

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AIC23 AUDIO CODEC

Line In

J19
LINE_IN_RING R61 4.70K, 1% RLIC C56 0.47uf
LINE_IN_TIP R62 4.70K, 1% LLIC C57 0.47uf
SJ_3515N
R63 4.70K, 1%
R64 4.70K, 1%

J42
MIN
R106 10.0K, 1%
R107 4.70K, 1% MICR
R108 10.0K, 1%
C107 1.0uf
C108 47p
SJ_3515N

Line Out

J20
LINE_OUT_RING
LINE_OUT_TIP
SJ_3515N
R65 100 RLOC C63 0.47uf RLINEOUT
R66 100 LLOC C64 0.47uf LLINEOUT
R67 47.5K 1%
R68 47.5K 1%

Amplified Line Out

J21
PHONES_OUT_RING
PHONES_OUT_TIP
SJ_3515N
C68 220uF
C69 220uF
R69 47.5K 1%
R70 47.5K 1%

AIC_SPI_CS [2] AIC_SPI_CS
AD_SDIO [2,3,4] AD_SDIO
AD_SCLK [2,3,4] AD_SCLK

AIC_DOUT [2] AIC_DOUT
AIC_DIN [2] AIC_DIN
AIC_LRCIN [2] AIC_LRCIN
AIC_LRCOUT [2] AIC_LRCOUT
AIC_BCLK [2] AIC_BCLK
AIC_XCLK [2] AIC_XCLK

3.3V
AIC_SPI_CS R57 4.70K, 1%
AD_SDIO R58 4.70K, 1%
AD_SCLK R59 4.70K, 1%
AUDIO_MODE R60 4.70K, 1%

U5
RLINEIN 19 RLINEIN
LLINEIN 20 LLINEIN
MIC_IN 18 MICIN
MIC_BIAS 17 MICBIAS
ROUT 13
LOUT 12
RALINEOUT 10 RHPOUT
LALINEOUT 9 LHPOUT
AIC23

BCLK 3 AIC_BCLK
CS_n 21 AIC_SPI_CS
SDIN 23 AD_SDIO
SCLK 24 AD_SCLK
MODE 22 AUDIO_MODE
DOUT 6 AIC_DOUT
DIN 4 AIC_DIN
LRCIN 5 AIC_LRCIN
LRCOUT 7 AIC_LRCOUT
CLKOUT 2
XTO 26
XTI.MCLK 25 AIC_XCLK
AVDD 14 3.3V_AUDIO
VMID 16 AIC_VMID
AGND 15
HPVDD 8
HPGND 11
DVDD 27
BVDD 1
DGND 28

L3 120ohm, 800mA
3.3V
C58 1.0nF
C59 0.1uf
C60 10uF
C61 0.1uf
C62 10uF
C65 1.0nF
C66 0.1uf
C67 10uF

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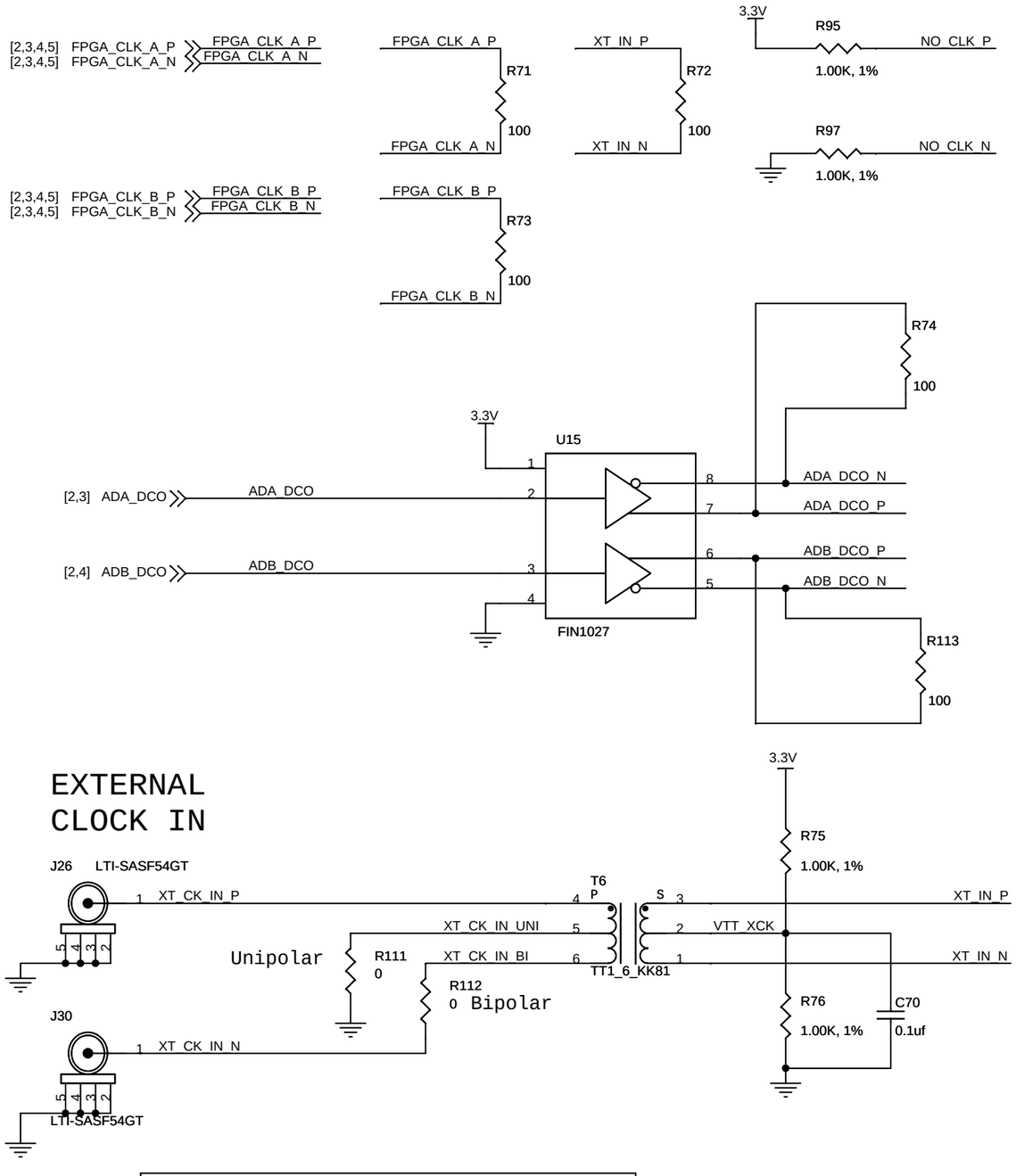

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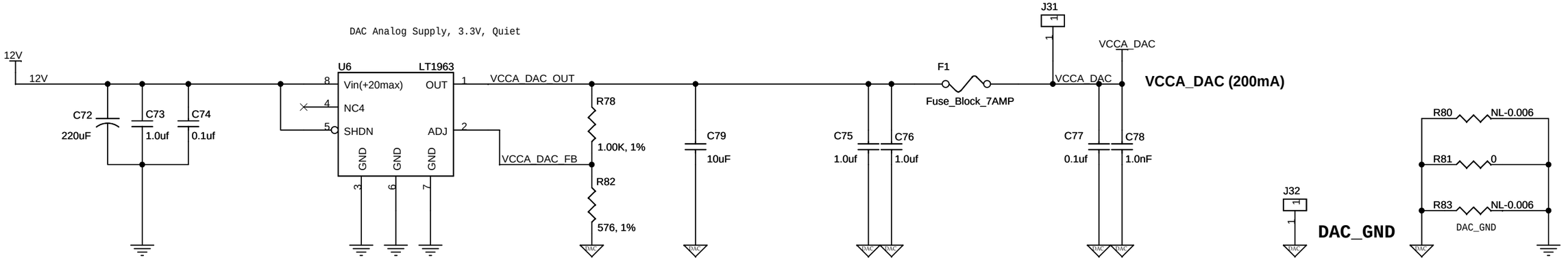
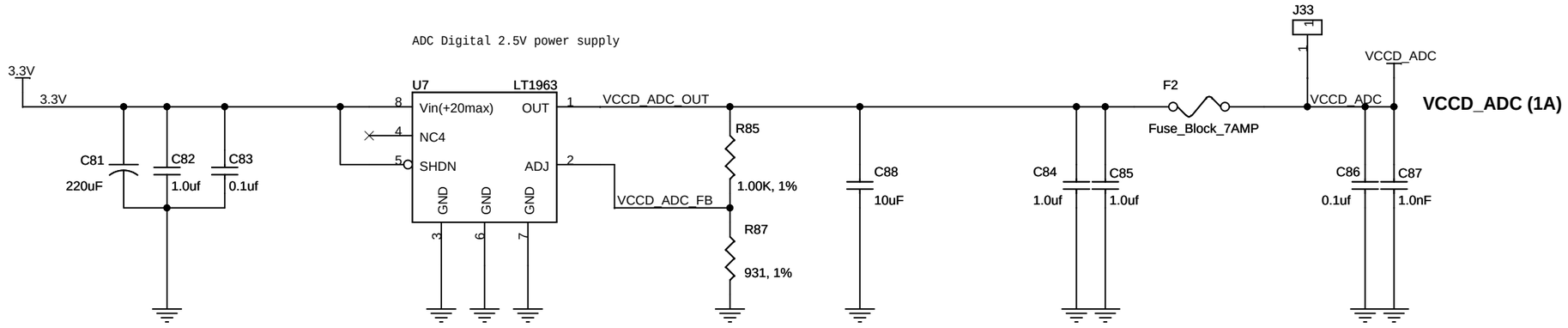
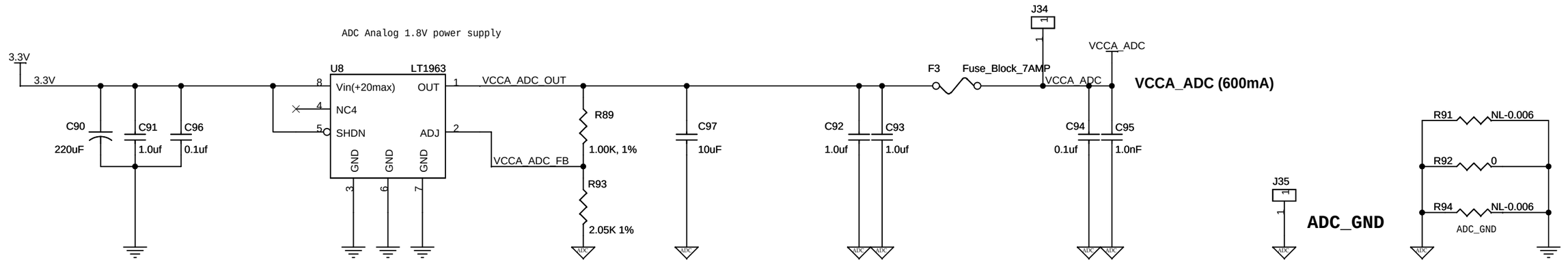
DAC Analog Supply, 3.3V, Quiet



ADC Digital 2.5V power supply



ADC Analog 1.8V power supply



Note: Each LT1963 Regulator has at least one square inch of copper on top and bottom layers for power dissipation.

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